Analysis of the Applicability of Reconfigurable Computers in Satellite Telemetry Data Processing

Kenneth B. Winiecki, Jr.
Lockheed Martin Space Mission Systems & Services

Marco A. Figueiredo
Stinger Ghaffarian Technologies, Inc.

Terry L. Graessle
Lockheed Martin Space Mission Systems & Services

Parminder S. Ghuman
National Aeronautics and Space Administration

Photonics East
#3526–06
November 2, 1998

ASDP
Adaptive Scientific Data Processing

Goddard Space Flight Center
Microelectronics and Signal Processing Branch

Overview

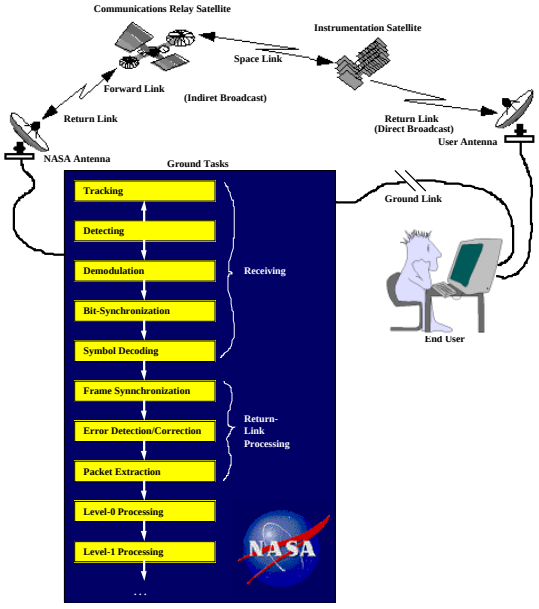
ASDP

- Goal
- Background: A NASA Processing Challenge
  - remote-sensing satellite telemetry data processing
  - the EOS-AM1 spacecraft and MODIS instrument
- Tasks
  - code and hardware selection
  - implementation and results
- Observations
- Conclusions
- For Further Information

Goal

Examine the utility of applying commercial, off-the-shelf (COTS) reconfigurable computing technology and tools to NASA telemetry data processing within a short (6-month) timeframe.

Remote-Sensing Satellite Telemetry



Ground-Based Processing

ASDP

- Receiving
  - tracking, detection, demodulation, bit-synchronization, symbol-decoding
  - well-accommodated in real-time by software and special-purpose hardware
- Return-Link Processing
  - frame-synchronization, error detection/correction, packet extraction
  - well-accommodated in real-time by software and special-purpose hardware

Ground-Based Processing

(cont'd)

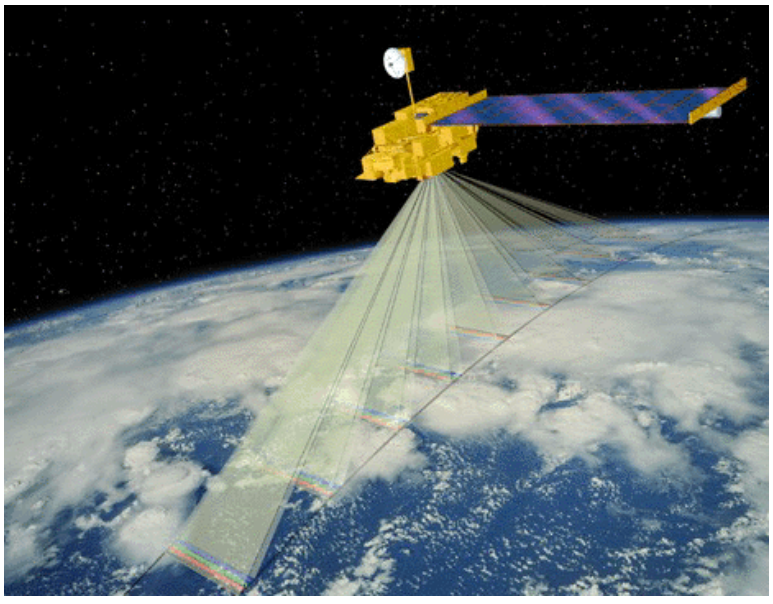
ASDP

- Level-0 Processing
  - packet stream separation and reconstruction
  - performed in batch-mode by software
    - » mission-specific: not suitable for special-purpose hardware
    - » highly I/O-bound: not suitable for reconfigurable computing
- Level-1 Processing
  - data stream (image) reconstruction, geolocation, calibration
  - performed in batch-mode by software
    - » instrument-specific: not suitable for special-purpose hardware
    - » some compute-bound tasks suitable for reconfigurable computing

Ground-Based Processing
(cont'd)

- Level-2 through Level-N Processing
  - data interpretation, data product generation
  - performed in batch-mode by software
    - » end-user-specific: not suitable for special-purpose hardware
    - » highly compute-bound: suitable for reconfigurable computing

EOS-AM1 Spacecraft with MODIS Instrument



EOS-AM1 Spacecraft

EOS-AM1: Earth-Observing System Ante-Meridian 1

- launch scheduled for May 1999
- will generate 1 TB (terabyte = 10^{12} bytes) of telemetry data per day
- will double the current NASA earth-science data in 5 months
- will generate 2 PB (petabyte = 10^{15} bytes) of data over its 6-year life
- platform for 5 instruments
  - » Advanced Spaceborne Thermal Emission and Reflection Radiometer (ASTER)
  - » Clouds and the Earth's Radiant Energy System (CERES)
  - » Multi-angle Imaging Spectroradiometer (MISR)
  - » Moderate-Resolution Imaging Spectroradiometer (MODIS)
  - » Measurements of Pollution in the Troposhpere (MOPITT)

MODIS Instrument

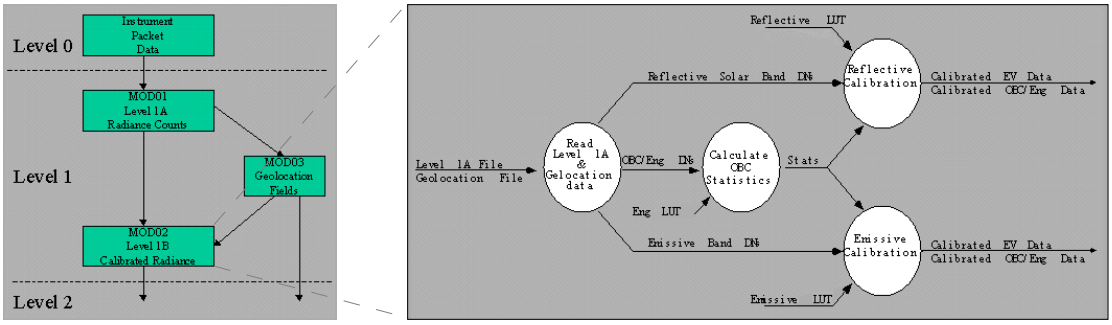
MODIS: Moderate-Resolution Imaging Spectroradiometer

- scans Earth every 1.447 s, covers the entire surface every 2 days
- each scan contains 36 Earth-view images, one for each of 36 distinct bands of the electromagnetic spectrum from far-infrared through visible, plus a small number of calibration-source-view images
- each Earth-view image is 2200 km long and varies from 10 km wide in the middle to 25 km wide at the ends
- images range from 1354 x 10 pixels (1000 m resolution) to 5416 x 40 pixels (250 m resolution); over 1 M pixels per scan
- all pixel values are 12 bits

Tasks

- Study existing code and select fragment to accelerate
- Survey COTS technology and select hardware and development tools
- Design, implement and test a hardware-accelerated version of the code
- Evaluate and demonstrate the solution

MODIS Level-1 Processing



Code Selection

- Level-1: the most universal processing level containing suitably compute-bound tasks
- Level-1B: the most compute-bound Level-1 code module
- Reflective Calibration: the most compute bound Level-1B task, and the largest task that was estimated could be accommodated with the given resources

Hardware Selection

- SGI Origin 200 Server: lowest-cost SGI with PCI bus (existing code written in C for SGI Challenge)
- Annapolis Microsystems' WildForce PCI Reconfigurable Computer: contains 180k gates

Implementation

- Used FPGA logic design tools from Xilinx and Synopsys, and designed only in VHDL
- Pipelined architecture produced one result per 30 MHz clock cycle
- Designed a fixed-point implementation of the floating-point algorithm from the code
- Development details contained in “Adaptive Scientific Data Processing – Fall 1997 Report” available on-line (reference on last page)

Results

```
------------------------------------------------
Initializing software-based L1A-to-L1B program....
Total program time:                     49.26 s
Reflective_Cal time:                    16.51 s
------------------------------------------------
Initializing FPGA-based L1A-to-L1B program....
Total program time:                     39.45 s
Reflective_Cal time:                     1.78 s
------------------------------------------------
Software-based Reflective_Cal fraction:  33.52 %
FPGA-based Reflective_Cal fraction:       4.50 %
Speed multiple:                           9.28 X
------------------------------------------------
```

- Test data set contains 10 scans
- Reflective Calibration processing time dropped 89%, running at more than 9 times the original speed
- Reflective Calibration portion of total processing time dropped 87%, thus ceasing to be a bottleneck

Observations

- Application of RC requires hardware and software engineering skills – i.e., computer engineers
- The ideal RC development tool should accommodate the computer engineer by integrating:
  - design specification in a high-level graphical/symbolic language instead of hardware symbols or hardware description languages
  - partitioning of a design among devices and systems
  - design of configuration overlays (for dynamic reconfiguration)
  - implementation
  - testing and analysis

Observations *(cont'd)*

- For high-bandwidth host-platform-driven applications, RC products must provide a host interface and driver design which avoids I/O bottleneck
- RC products ought to provide more forward-compatibility to accommodate FPGA product evolution

Observations *(cont'd)*

- 1997 RC technology offered 36 k gates per FPGA device and 40 MHz clock speeds; 1998: 85 k gates, 50 MHz; 1999: 1 M gates?...
- "Reconfigurable computing (RC) is the smallest segment of the FPGA market, but has exhibited sustained growth and is recognized as having the greatest potential"

Conclusions

- Demonstrated nearly an order-of-magnitude improvement in processing speed on one NASA telemetry data processing task in a relatively short time using COTS RC technology and tools
- Indicated that great potential value exists in RC to NASA processing needs
- RC technology seems to be "ripe" for some tasks, still "green" for others

Conclusions *(cont'd)*

ASDP

- Enormous room for improvement exists in RC development tools, RC design, and FPGA design
- Several efforts are underway to address RC application obstacles, funded by the Defense Advanced Research Projects Agency (DARPA) Adaptive Computing Systems study
- The ASDP group at NASA GSFC provides an interface between NASA RC efforts and the research community

For Further Information

ASDP

Visit the ASDP Website: http://fpga.gsfc.nasa.gov/

ASDP
Adaptive Scientific Data Processing